*Keyword:* [Designator Pin List]

*Required:* Yes

*Description:* Defines the pin names of the designator pins. It also defines which designator pins are connected to power and ground. Designators are defined in the [EMD Designator List] section and can be instances of either an .ibs [Component] or an .emd [Begin EMD].

*Sub-Params:* signal\_name, signal\_type, bus\_label

*Usage Rules:* Following the [Designator Pin List] keyword are three columns. The first column lists the pin name (in a device data book this can also be called pin number). The pin\_name shall be preceded by the reference designator followed by a “.” (e.g. U2.DQ1).

The second column lists the name of the signal associated with the pin\_name. This signal\_name is the name that is assigned by the top-level EMD and may be reassigned from the signal\_names of the designator .ibs [Component] or of the designator .emd [Begin EMD]. This allows attached components or attached electrical module descriptions with standardized pin\_name positions but with different manufacturer terminology to be interchanged.

The third column is required if the pin is a rail pin or a no connect pin.

The allowed values for this third column are:

POWER - reserved model name, used with power supply pins

GND - reserved model name, used with ground pins

NC - reserved model name, used with no-connect pins

Note, “NC” is sometimes used for non-digital pins that cannot be described by IBIS functions.

The fourth column, bus\_label, is optional for rail pins (signal\_type POWER or GND). The bus\_label entry is a name assigned to a subset of the pins with a rail signal\_name.

The optional bus\_label entry provides a way to describe some routing groupings such as left- and right-side rail paths. If the bus\_label column is not specified for signal\_type POWER or GND, then the bus\_label shall be assumed to be the signal\_name.

The [Designator Pin List] keyword shall be followed by the strings “signal\_name”, “signal\_type”, and “bus\_label” as column headings.

Pin names must be the alphanumeric external pin\_names of the designator. The pin names cannot exceed eight characters in length. In addition, “NC” is a legal signal\_type and indicates that the pin is a “no connect” (or when there is no model available for it). As described in Section 3.2 the reserved words “GND”, “POWER”, and “NC” are case-insensitive.

Note that all EMD Pins and Designator Pins that have the same signal\_name (or subset bus\_label) are “connected”. Connection details between the EMD Pins and any Designator Pins are described by the electrical models under the [EMD Model].

All pin\_name pins are required to be listed. The signal\_name entry may be assigned to designate pins on .ibs [Component]s or .emd [Define EMD] that are associated with corresponding [EMD Pin List] pins. In other words, the [EMD Pin List] pin\_names may be different than the corresponding pin\_names of the designator component, but the EMD-level assigned signal\_name entries are used for the association. Identical signal\_name entries are permitted for the same designator to indicate shorted terminals at the specified designator (for example, to document a 1-to-many layout topology). This association will be useful for I/O pins when describing Aggressor\_Only terminals discussed later.

Each non-rail pin\_name pin (generically referred to as I/O pins) shall have only a signal\_name entry. For I/O pins, no signal\_type or bus\_label entry is permitted.

*Example:*

| A SIMM Module Example:

|

[Begin EMD] 16X8\_SIMM

[Manufacturer] Quality SIMM Corp.

[Number Of EMD Pins] 6

[EMD Pin List] signal\_name signal\_type bus\_label

A1 VSS GND

A2 DQ1 | I/O pin

A3 DQ2 | I/O pin

A4 VDD POWER VDD1

A5 VDD POWER VDD2

A6 VDDQ POWER

[End EMD Pin List]

[Designator Pin List] signal\_name signal\_type bus\_label

U1.11 VSS GND

U1.12 DQ1 | I/O pin

U1.13 DQ2 | I/O pin

U1.14 VDD POWER VDD1

U2.21 VDD POWER VDD2

U2.22 DQ1 | I/O pin

U2.23 DQ2 | I/O pin

U2.24 VDDQ POWER

[End Designator Pin List]

Page 36, Rules 1a, , iii and iv:

* + 1. Within each [EMD Model], <designator>.<pin\_name> and their corresponding signal\_name entries (as listed in the [Designator Pin List] keyword) shall be distinct for I/O pins
    2. At any one interface and for all [EMD Model]s referenced by all [EMD Set]s under an [EMD Group], no duplicate pin\_name entries are permitted for I/O pins

Proposed Revision for iii and iv.

* + 1. Within each [EMD Model], <designator>.<pin\_name> and the corresponding signal\_name entries (as listed in the [Designator Pin List] keyword) can be distinct or identical for I/O pins
    2. At any one interface and for all [EMD Model]s referenced by all [EMD Set]s under an [EMD Group], no duplicate pin\_name entries are permitted for I/O pins
    3. A single [EMD Model] shall contain all of the I/O terminals that describe all of the I/O nets. (Splitting the [EMD Model] into several connected I/O [EMD Model]s is not permitted.) However, parts or all of the rail terminals in section 2. below can be expressed in separate [EMD Model]s.